REMARKS

In an Office Action mailed February 11, 2004, claims 1-26 were rejected under 35 U.S.C. 103(a) over U.S. Patent No. 5,394,524 (DiNicola) in view of U.S. Patent No. 6,275,239 (Ezer) and further in view of U.S. Patent No. 6,208,350 (Herrera). In response thereto, Applicants amend claims 1, 7, 14, 20, and 26, present new claims 27-30 for the Examiner's consideration, and respectfully request the reconsideration of claims 1-30 and the allowance thereof, thereby placing the application in condition for allowance.

The Examiner stated that it would have been obvious to substitute media coprocessor 102 of Ezer (which can be programmed to perform several 2D or 3D image processing functions) for attribute processor (AP) 306 of DiNicola. The Examiner also stated that it would have been obvious to combine the mode selection of Herrera to arrive at the invention of claims 1 and 7. The Examiner further reasoned that it would have been obvious to one of ordinary skill in the art to combine the teachings of DiNicola, Ezer, and Herrera to arrive at the features of each of the remaining claims.

However the combination of the three references, even if it would be obvious to combine them in the manner stated, in no way shows or suggests the invention as presently claimed in claims 1-30. According to claim 1, for example, an image processing system comprises a two-dimensional image pipeline and a three-dimensional image pipeline each of which have a plurality of stages including a first stage and a last stage. The claimed image processing system also comprises dual-mode sub-processing circuitry operable in a two dimensional mode at an intermediate stage of the two-dimensional image processing pipeline and in a three dimensional mode at an intermediate stage of the three-dimensional image processing pipeline.

The image processing system of claim 1 has the advantage of creating virtual pipelines that appear to process data through multiple stages in a manner appropriate to their particular specialty, but which in fact uses common circuitry at an intermediate stage that can be selectively placed in one mode or another, resulting in efficient use of the inherent symmetries in the pipelines, and thereby reducing the overall number of functional units, and chip area or board space required to support them (page 5, lines 9-16).

On the other hand DiNicola's AP 306 performs preprocessing of graphics data in either 2D or 3D format before the data has been committed to either 2D subsystem 301 or to 3D subsystem 303 (col. 5, lines 55-59). Substituting media processor 102 of Ezer for DiNicola's AP 306 (assuming it would be obvious to do so) would not produce the claimed invention. This combination would at most only show processing either 2D or 3D data before the image processing circuitry has been separated into specialty hardware. Once this separation has occurred, DiNicola processes data concurrently in separate subsystems.

The image processing circuitry of the invention of claim 1, however, includes dual-mode sub-processing circuitry that operates to perform graphics processing operations on data that has already been processed in and is already part of either a two-dimensional image processing pipeline or a three-dimensional image processing pipeline. DiNicola does not process 2D image data in specialty 2D processing circuitry or 3D image data in specialty 3D image processing circuitry until after AP 306 has formatted the data.

Each of the remaining independent claims recites similar features. Claim 7 recites a method for use in image processing circuitry having a two-dimensional image pipeline and a three-dimensional image pipeline each having a plurality of stages including a first stage and a last stage. The method includes steps of performing motion compensation operations associated with the two-dimensional image pipeline at an intermediate stage thereof and performing rasterization operations associated the three-dimensional image pipeline at an intermediate stage thereof using the dual-mode sub-processing circuitry. These elements are not shown or suggested by the combination of DiNicola, Ezer, and Herrera.

Claim 14 recites mode control circuitry for use in an image processing system having a two-dimensional image pipeline and a three-dimensional image pipeline each having a plurality of stages including a first stage and a last stage. The mode control circuitry includes dual-mode sub-processing circuitry that in a two-dimensional mode performs motion compensation operations associated with the two-dimensional image pipeline at an intermediate stage thereof and in a three-dimensional mode performs rasterization operations associated with the three-dimensional image pipeline at an intermediate stage thereof. These elements are not shown or suggested by the combination of DiNicola, Ezer, and Herrera.

Claim 20 recites a method for use in an image processing pipeline having a two-dimensional image pipeline and a three-dimensional image pipeline each having a plurality of stages including a first stage and a last stage. The method includes the step of controlling the dual mode sub-processing circuitry to perform either motion compensation operations associated with the two-dimensional image pipeline at an intermediate stage thereof in a two-dimensional mode, or rasterization operations associated with a three-dimensional image pipeline at an intermediate stage thereof in the three-dimensional mode. These elements are not shown or suggested by the combination of DiNicola, Ezer, and Herrera.

Claim 26 recites a media processing system having a two-dimensional image pipeline and a three-dimensional image pipeline each having a plurality of stages including a first stage and a last stage, and dual mode sub-processing circuitry operable to perform either motion compensation operations associated with the two-dimensional image pipeline at an intermediate stage thereof in a two-dimensional mode, or rasterization operations associated with a three-dimensional image pipeline at an intermediate stage thereof in a three-dimensional mode. These elements are not shown or suggested by the combination of DiNicola, Ezer, and Herrera.

Claim 27 recites a processing apparatus comprising first and second specialty pipelines each having a plurality of stages including a first stage and a last stage, and dual mode sub-processing circuitry operable in a selected one of first and second modes wherein in the first mode the dual-mode sub-processing circuitry forms an intermediate stage of the first specialty pipeline and in the second mode the dual-mode sub-processing circuitry forms an intermediate stage of the second specialty pipeline. These elements are not shown or suggested by the combination of DiNicola, Ezer, and Herrera.

The combination of DiNicola, Ezer, and Herrera, even if it were obvious to combine them in the manner stated by the Examiner, does not result in the invention claimed in any independent claim. Thus for at least this reason the claims are allowable and Applicants respectfully request the allowance of the present application.

If, for any reason, the Office is unable to allow the Application on the next Office Action, Applicants request a telephone interview to help resolve any remaining issues.

The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 01-0365.

Respectfully submitted,

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Date

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